SONOS EMBEDDED MEMORY WITH CVD DIELECTRIC

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ABSTRACT

An embedded semiconductor memory is fabricated by: forming diffusion bit line regions in a semiconductor substrate; then thermally oxidizing the upper surface of the substrate, thereby forming a bottom oxide layer over the substrate and simultaneously forming bit line oxide regions over each of the diffusion bit line regions; and then forming an intermediate dielectric layer (e.g., silicon nitride), over the bottom oxide layer and the bit line oxide regions. CMOS well implants are then performed in a CMOS section of the device through the silicon nitride layer and bottom oxide layer. The silicon nitride layer and bottom oxide layer are then removed in the CMOS section, and a top dielectric layer, such as a high-temperature oxide or a high-k dielectric, is deposited. The top dielectric layer completes a memory stack of the memory device, and forms a gate dielectric layer of a high voltage transistor in the CMOS section.